# 1 Project details

## 1.1 Application team

Dennis Furey, Plumstead Publishing House, Ltd.

## 1.2 Application details

The project title is “Design Automation for Delay Insensitive Circuits”, the start date is June 1, 2020, and the duration is eighteen months. This application is not a resubmission.

## 1.3 Research category

The research category is **industrial research**.

## 1.4 Project summary

In brief, this project is about gaining the traction that has previously eluded asynchronous circuit development by changing people’s minds about it. While this topic has endured a range of approaches, this project is a bet on a particularly systematic one, namely delay insensitive design, to attract hobbyists and educators. These groups are the least locked in to industry standard methodologies and so the best chance for a small scale project to have an outsized long term influence. The result of this project will be a minimal suite of free software tools empowering users to design, synthesize, and verify simple delay insensitive circuits in terms of pristine abstractions that demand no prior specialist or interdisciplinary knowledge.

Being impossible to build from standard logic gates, delay insensitive circuits have always depended on custom libraries of primitive components for functional completeness. Previously proposed libraries have required primitives having up to eight connecting terminals, but even the best known solutions have needed some with at least five. Complex primitives are detrimental to efficient routing and connectivity, especially for integrated circuits with repetitive array layouts, in which a square cell with one terminal on each side is ideal. They also complicate the algorithms required for EDA software. However, a recent publication by the principal investigator shows that all delay insensitive circuits actually can be built from seven suitably chosen primitives having at most four terminals each (*Delay Insensitive Circuits : Structures, Semantics, and Strategies*, Plumstead Publishing House, 2019). This new result settles a long standing open question and has yet to be exploited anywhere.

A further innovation will be the implementation of a novel circuit synthesis algorithm, also first published in the above mentioned work and not yet deployed elsewhere. Circuit synthesis generally refers to the problem of translating an intuitive description of an unknown circuit’s desired behavior to a listing of components and a road map for their connecting wires to realize the behavior, in effect designing the circuit automatically. The new algorithm employs a behavioral description in terms of an asynchronous process model that relieves the user of any concern for timing events, state variables, connection topology, or restrictive assumptions about the environment or manufacturing technology. It also avoids the common pitfalls of exponential time or memory usage by a rigorous divide-and-conquer strategy, and

where possible it applies some of the same circuit optimizations that an expert human designer would apply.

## 1.5 Public description

As the circuits used in our phones and other technology become more complex and sophisticated with each new generation, effective ways of designing them easily and correctly become more crucial than ever to their trustworthiness and energy efficiency. This project advances a promising methodology based on a theoretical foundation of delay insensitive circuit design that is well understood, but whose takeup in industry until now has been undermined by limitations of standard electronic design automation software and tooling, and regrettably also by cultural inertia.

Common practice inures us to computers and internet connected devices spending most of their lives idling while they wait for relatively infrequent external events or input signals, and wasting energy even when idle by punching a clock billions of times each second. To make matters worse, they must also incorporate all of the wiring needed to connect the clock to every component within, all at considerable cost, as only the most basic prerequisite to accomplishing anything visibly useful. For historical reasons, computers and related hardware have been designed according to this paradigm for seventy years.

Improved energy efficiency alone may justify getting rid of the clock in everything from battery powered devices to large data centers, but among other potential advantages, doing so makes circuits formally verifiable, resistant to certain side-channel cryptographic attacks, tolerant of greater variations in the manufacturing process or operating conditions, and conducive by their modularity to smooth upgrade paths. On the other hand, progress in this direction is stalled by a threefold vicious cycle: reticence among engineers over the perceived difficulty of delay insensitive (clock free) circuit design, avoidance of this topic by standard engineering curricula, and its consequent neglect by *de facto* standard electronic design automation software.

As a first step toward dismantling these barriers, a minimal suite of software tools supporting synthesis and verification of delay insensitive circuits as a proof of concept will be the main result of this project. Built around a circuit description language of a simplicity afforded by a mature body of theory, these tools will be usable productively even by novice circuit designers and students. A further emphasis of this project therefore is to engage with educators and the community by freely distributing the software including full source code, documentation, and tutorial materials under permissive licenses through an actively maintained web presence.

## 1.6 Scope

Many innovative projects about integrated circuits and semiconductor devices have been funded in previous Innovate UK competitions, especially for improving energy efficiency, but the key enabling technology of electronic design automation (EDA) software is distinctly under-represented with scarcely more than a few instances to be found. Yet, the economic benefit of any hard won advances in circuit materials and manufacturing remains partly untapped without commensurate advances in engineering capability and productivity. As a neglected topic with a growing legacy of unchallenged assumptions, design automation is

poised for disruption in line with the competition brief, and it diversifies the grant portfolio at relatively low cost.

There are at least four good reasons to call the proposed project a “game changer” in the EDA business.

- Engineers and most academics have been complaining for years that nobody can figure out how to design asynchronous circuits or that doing so is too hard. This project will make that position untenable to an informed and honest observer.
- As a result of this project, lower power dissipation than what is possible for conventional synchronous circuits will be available for the taking to anyone bold enough to retool.
- An ample lead time to develop this software is all but guaranteed as long as the big electronics companies are free to choose between dedication to their established customer base and a wild foray into uncertain emerging markets hinging on unconventional ideas.
- The rigorous theoretical foundations for delay insensitive circuit design raise the bar in one stroke for specification, verification, optimization, scalability, and performance analysis, eliminating many of the opportunities for bugs, glitches and bottlenecks that plague conventional synchronous circuits.

# 2 Application questions

## 2.1 Need or challenge

- The digital circuitry in every phone, tablet, computer, medical instrument, or vehicle dashboard affects all of our lives, but its design and development tend to be dominated increasingly by an oligopoly of large American and Asian companies. The core motivation for this project is to open the market to genuine competition from less established but potentially more innovative participants by easing the technological barriers to entry.
- The major vendors of electronic design automation tools (Cadence, Mentor Graphics, Synopsys) and FPGA development suites (Intel/Altera, Lattice Semiconductor, Xylinx) evidently deem it safe to ignore the educational and hobbyist hardware developer markets. The high licensing costs and steep learning curves of proprietary offerings are likely to leave this space wide open to any moderately innovative company for the foreseeable future.
- Cost savings are possible through free software design tools (KiCad, gEDA, Yosys, nextpnr, Verilator, Icarus, SymbiFlow) and open source FPGA development kits (iCEBreaker, ULX3S). Various third party prototyping boards (Papilio, TinyFPGA, *etc.*) package low end proprietary FPGA chips from the major vendors whose specifications have been reverse engineered no thanks to the vendors. However, these solutions tend to lag the top of the range. Reverse engineering efforts (*e.g.*, Project X-Ray) are subject to obsolescence whenever the FPGA vendors decide to change their proprietary specifications or discontinue them. Moreover, by imposing similar methodologies to those of traditional proprietary offerings, open source language based or graphical development tools as conceived until now impose similar cognitive burdens on the designer.

- This project focuses on exploring an alternative paradigm of electronic design automation based on the theory expounded in the recently published textbook *Delay Insensitive Circuits : Structures, Semantics, and Strategies*, whose author is the principal investigator. As a mature research area with an active community spanning academia and industry, it may take only a small additional impetus under the right circumstances to achieve mainstream status.

- The cultural challenge to this opportunity stems from a dogma decreed almost from day one in engineering education and seldom reappraised thereafter: all practical circuits need a timing signal wired from a central source to each and every component to ensure they march step-by-step in unison, or else chaos would reign. For students and professionals alike, training and tool support relentlessly reinforce this notion as a universal organizing principle. Whatever the cost in materials, performance, power dissipation, or design effort, the alternative is almost never considered.

## 2.2 Approach or innovation

- The priority in responding to this need is to dispel the perception of unclocked circuits being impractical, inscrutable, or unimaginable, by a simple demonstration to the contrary. Unlike the decades-long accumulated legacy of proprietary tooling and its derivatives, a workflow built on a straightforward delay insensitive circuit description language can be taught to novice designers no more arduously than an introductory programming lesson.

- When artificially imposed timing conditions are jettisoned, they take a multitude of common stumbling blocks with them. Circuits become more modular and their modules more interchangeable without tedious retrofitting. Questions of correctness and compatibility become unambiguous and possible to settle computationally. The designer is freed to understand the circuit in terms of causal relationships rather than the rise and fall of every individual timing signal. These features improve on the state of the art by boosting the productivity of circuit designers of any ability and enabling more ambitious projects.

- This approach is disruptive insofar as industry standard FPGA technology would need certain minor enhancements before it could support the components used in delay insensitive circuits. This issue in principle does not affect custom silicon regarded as a blank slate, but most likely precludes the use of any existing standard cell libraries or IP blocks.

- The principal investigator is free to undertake this project unencumbered by any prior legal, contractual, or financial obligations, and acts with full executive authority and voting control of Plumstead Publishing House, Ltd..

- The company's current product line consists of the textbook *Delay Insensitive Circuits : Structures, Semantics, and Strategies* in hardbound and ebook formats. The book will serve as a companion reference and theoretical primer for the software resulting from this project.

- An immediate competitive advantage will be the expansion of the publishing catalog to a broad audience of educational and hobbyist customers, with a view in the long term to industrial customers. Because circuit verification becomes computationally intensive for large systems, a possible future revenue stream may come from cloud based verification as a service using distributed parallel algorithms.
- A minimum viable tool suite using a delay insensitive circuit description language is the intended output from this project, if not to an industrial standard then at least to that of a teaching aid and proof of concept. By automating much of the workflow, this result will effect a clear and accessible demonstration of the feasibility of delay insensitive circuit design.

## 2.3 Team and resources

- The principal investigator Dennis Furey will be responsible for all aspects of the project, including software output, system administration, web development, and accounting.
  - 1985 B.S. Computer Engineering, Rochester Institute of Technology
  - 1990 M.Sc. Computer Science. New York University
  - 1994 Ph.D. Computing, Imperial College
  - 1996-1998 postdoctoral researcher in asynchronous circuits, Queensland University of Technology
  - 1998-2000 senior research fellow in concurrent systems, London South Bank University
  - 2003-2004 quantitative software developer, Vantage Derivatives
  - 2006 visiting faculty member, California Institute of Technology
  - 2010-2011 web developer, Proper Computing
  - 2011-2012 technical writer on FPGA products, Maxeler Technologies
  - 2013-present independent author and publisher, Plumstead Publishing House, *Delay Insensitive Circuits : Structures, Semantics, and Strategies*
- Equipment, resources, and facilities consist of a single high end GNU/Linux workstation on site and Amazon Web Services accessed remotely via broadband connection for backups, web hosting, and distributed computing.
- There are no external parties or subcontractors.
- There are no other project partners.
- There are no roles in need of recruitment. However, participation from the free software community will be welcome though not essential, and will be enabled by the Github platform. Cultivating relationships in a geographically distributed and neuro-diverse talent pool is an important step toward effective recruitment to build the company in the future after this project.

## 2.4 Market awareness

This project pertains in the long term to the global semiconductor market, for which quantitative data are well known, and in the short term to an emerging market of UK educators and hobbyists that is more difficult to quantify.

- According to IBISWorld report C26.110 from March 2019, the UK semiconductor sector is in decline due to foreign competition despite strong global demand, in contrast to its growing American and Chinese counterparts. Revenues of £1.949 billion in 2019 are down from £2.019 billion in 2018, and are expected to fall further to £1.900 billion in 2020. UK exports in the sector show an average annual decline of 3.8% over five years with imports increasing at a similar rate, especially from Germany and America. The American semiconductor manufacturing sector is worth $55 billion and the Chinese $148 billion.

- There are 20,000 schools in the UK sharing an £80 million government grant earmarked for computing education over the coming four years from the NCCE professional development program. 70,000 students took the GCSE in Computer Science in 2018, up from 4,000 in 2013.

Semiconductor manufacturers' business models are based either on operating their own fabrication facilities or being "fabless". The latter entails outsourcing the manufacture of their proprietary circuit designs, especially to Asia, for lower wages and for the avoidance of an initial capital outlay on the order of $3 billion to build a fab. Newport Wafer Fab Ltd. and Seagate Technology PLC both continue to operate UK facilities at present. Incumbents work hard to maintain a barrier to entry through patent "protection" and a culture of secrecy.

## 2.5 Outcomes and route to market

- The company's current position is that of a book publisher. This project will establish a position as software publisher.

- The target customers are educators and hobbyists. They will use the software for teaching or experimentation.

- The route to the market is by collaborating with teachers on school activities or lessons, participating in technology meetups or user groups, and maintaining an active web presence.

- By creating awareness and interest in an alternative approach to digital circuit design, this project will create demand for the hardware needed to put it into practice. Private investment and recruitment subsequent to the completion of this project will enable the company to profit from hardware sales.

- In the short term, there will be no effect on the company's productivity because it is not yet in the hardware business. In the long term, the project will enable the recruitment of developers and engineers having some prior familiarity with the subject area, thereby enabling a team effort to expand the product line with shorter times to market.

- At this stage, raising awareness of these innovations is a bigger problem than "protecting" them, hence the initial strategy of free software distribution. By the time the market grows enough for established players to take notice, the company's business model will have diversified in two ways. One is to offer cloud based circuit verification or optimization as a service using advanced concurrent distributed algorithms that need not be published, and the other is to develop and license IP blocks for customers to integrate into their products, for example to support industry standard protocols or signal processing operations. The company's know-how will make these services difficult for a latecomer to copy.

- Targeting the commercial market after the project is finished will be done by attending and presenting at academic conferences and industry trade shows.

## 2.6 Wider impacts

Current electronics industry leaders are neither short sighted nor technically inept, but have achieved success through careful attention to the demands of their most profitable customers. Custom hardware development amenable to non-specialists using free open source software tools, whose performance at least initially need not be cutting-edge or nanometer-scale, will eventually unseat the major players not by surpassing these core competences, but by gradually accumulating mindshare in an emerging market whose demands are different. The less adaptable established firms might attempt to postpone the inevitable by doubling down on their proprietary offerings, with technological progress bypassing them in the end as it always does. The UK economy would stand to gain by this outcome because the industry leaders are elsewhere. A few other predictions naturally follow.

- Custom or semi-custom hardware development in-house will become viable for a segment of UK businesses whose current options are either to outsource the job to specialist foreign entities or to settle for less competitive off-the-shelf solutions.

- A project to make digital circuit design more effective and accessible at the professional level has implications for secondary and even primary education in keeping with the government's NCCE initiative. Rating only a single bullet point in one stage of the official curriculum at present, this topic in future may warrant broader coverage.

- It is easy to envision a future class of university students balking at the prospect of tedious, abstruse, and purposely incompatible tool chains and formalisms for their engineering course work when their prior educational exposure to digital circuit design has been nothing but straightforward and enlightened. By voting with their feet, they would put pressure on curriculum reform in higher education as well.

- Some of those students subsequently will attain positions of influence in industry with recruitment needs of their own, potentially arresting or reversing the brain drain of engineers from the UK insofar as it becomes known as a hospitable place for techniques that are more up to date.

With regard to environmental impact, this project has none in itself, but it may effect some small influence toward reducing the carbon footprint of the world's data centers. According

to a recent International Energy Agency report, data center usage now stands at 198 TWh or 1% of global energy demand. This project promotes self-timed circuit design techniques, for which low power dissipation is an undisputed advantage.

## 2.7 Project management

Project management is especially simple due to there being only a single partner, who is accustomed to working independently on long term projects.

Anticipated development tools include C and Zig programming languages for performance critical code, LaTeX document preparation utilities, Git source control with frequent updates distributed via the Github web site, and whatever free open source software libraries that may prove convenient on a GNU/Linux development platform.

Remote backups will be stored using Amazon Web Services, which will also be the platform of choice for any required distributed computing facilities and for hosting the project home page.

Web development tools for the home page may include Bootstrap Studio or Pinegrow for the front end, and the Go programming language and libraries for any needed server side features.

A layered software architecture is envisioned with the main components listed roughly in order of precedence below, and documentation of all phases to take place concurrently with development.

- core data structures in support of delay insensitive processes, hierarchical networks and related algebraic transformations and optimizations
- strongly performance critical algorithms for model checking, design space exploration, and state enumeration, with possible consideration of cloud based distributed solutions
- moderately performance critical algorithms for circuit synthesis covering state based, direct mapped, and special purpose modules
- an intermediate interpretive language encapsulating the core abstractions for flexible treatment of less performance critical operations
- a user-facing front end circuit description language, with syntax directed translation targeting the intermediate form
- a user-facing drag-and-drop GUI schematic editor front end for pedagogical purposes

## 2.8 Risks

This project is immune to commercial, managerial, and regulatory risks. It is ethically and environmentally neutral, it is not contingent on any form of certification, and it does not rely on any resources other than basic utilities for its completion.

Low probability risks include a natural disaster or the death of the principal investigator with insufficient time to brief a successor during the eighteen month project duration. The former risk can not be mitigated, but the latter will be mitigated by a well documented and frequently updated public source code repository.

A medium probability risk is that of a rival group outside the UK getting up to speed on the published theory and attempting to exploit it. The disadvantage of this outcome is that its benefit to the UK economy is less direct, but the risk is mitigated mainly by the time needed for an outsider to master the subject area. An estimate on the order of one year for a professional engineer is based on informal correspondence with participants in the asynchronous mailing list following the initial announcement of the current reference on the subject published by the PI this past summer (*Delay Insensitive Circuits : Structures, Semantics, and Strategies*, Plumstead Publishing House, 2019). Lacking both the first mover advantage and anything in the nature of IP "protection", rival groups taking any interest at all in this area would face an uphill path toward funding from their respective agencies or senior management.

With regard to IP, patent trolling is a plausible risk because it demands no engineering talent or credible legal argument from a fittingly ruthless and well heeled adversary. This risk is mitigated by several factors. As noted above, essentially all theoretical foundations of the work are publicly disclosed already. To the extent such ideas are patentable at all, any future patents on them would be subject to invalidation due to prior art. Previously filed patents pertaining to asynchronous circuits exist but most are trivial or overly broad. Their relevance to the proposed project is tenuous at best, and in any case their time to expiration is finite. However, if worse comes to worst, these issues impede only the commercial aspirations of an investigator, not the project's ultimate contributions to knowledge and technological progress.

## 2.9 Added value

- Without public funding, the only form in which this project might go ahead is as a hobby on the part of the PI. Public funding would enable and oblige it to be a full time occupation.
- If the project is funded and completed successfully, the business will be in a strong position to attract private investment for upgrading the deliverable from an initial working prototype to a marketable product.
- Currently the company's only income is from book sales, which are insufficient to support a full time developer. The time horizon to a return on investment makes this project unattractive to private investors at its current stage, and can not be shortened by throwing money at it because recruiting a large team experienced in this subject area is impossible. If the application is unsuccessful, the project will be less actively promoted and significantly postponed, perhaps to be overtaken in due course by better resourced and more timely investigators elsewhere.
- R&D activity prior to this project has focused on establishing, documenting, and publishing a firm theoretical foundation. This project would change the nature of the activity to a more applied direction. The activity will also change from essentially an individual effort by the PI to a more collaborative one.